CLAIMS

1. A method for synchronizing a clock signal to a data signal, comprising the steps of:

(A) detecting an edge of said data signal;

(B) determining whether a position of said edge is within a zone; and

(B) if said edge is not within said zone, adjusting said clock signal towards said position of said edge.

2. The method of claim 1, wherein step (A) comprises the sub-step of:

(A-1) sampling a number of clock signals using said data signal.

3. The method according to claim 2, wherein step (A) further comprises the sub-step of:

(A-2) encoding a position of said edge.

4. The method of claim 1, wherein step (B) further comprises:

comparing an encoded position of said edge to a predetermined value.

5. The method of claim 3, wherein step (A) further comprises the sub-step of:

storing said encoded position.

6. The method of claim 1, wherein step (C) comprises the sub-step of:

incrementing a value in response to a first polarity.

7. The method according to claim 6, wherein step (C) further comprises the sub-step of decrementing said value in response to a second polarity.

8. The method of claim 1, wherein step (C) further comprises the sub-step of selecting a number of clock phases based upon said value.

9. An apparatus for synchronizing a clock signal to a data signal, comprising:

a detector configured to produce a value representing a position of an edge of said data signal based upon a state of said clock signal; and

control circuitry configured to adjust said clock signal when said position of said edge is not within a predetermined zone.

10. The apparatus of claim 9, wherein the control circuitry further comprises a storage element configured to store an encoded position of said edge.

11. The apparatus of claim 9, wherein said control circuitry further comprises an increment/decrement logic circuit configured to adjust a third value in response to said second value.

12. The apparatus of claim 9, wherein said clock signal comprises a plurality of phases.

13. The apparatus of claim 9, wherein said control circuitry selects one or said plurality of phases as a system clock.

14. An apparatus for synchronizing a clock signal to a data signal, comprising:

means for detecting an edge of said data signal;

means for determining whether a position of said edge is within a zone; and

means for adjusting said clock signal towards said position of said edge when said position of said edge is not within said zone.